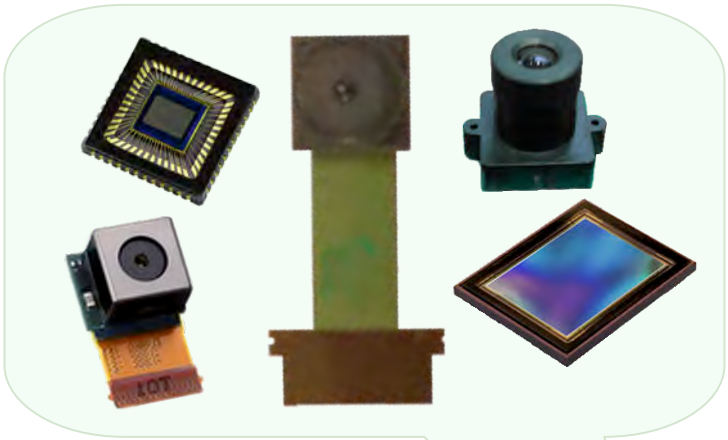
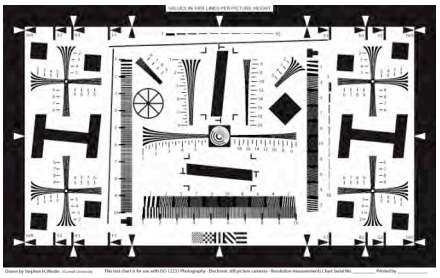
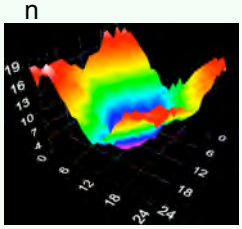
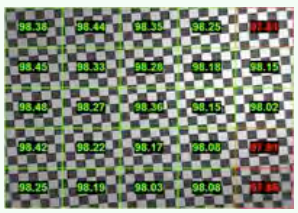
ISL-3200™ Digital Imaging Sensor Interface and Test Solution

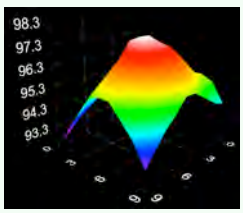




n







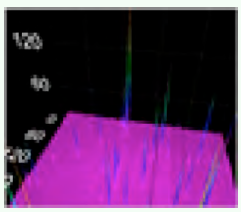


Table of Contents

1. INTRODUCTION

The ISL-3200™ is a cost-effective combination of sensor interface, test electronics, and application software that provides complete communications, image capture, and characterization testing, of a wide variety of image sensors. The ISL software application offers scripting and plug-in functionality, allowing enhanced graphical user interfaces to specific image sensor models as well as customized image processing analysis and characterization testing routines. The ISL software application is pre-configured with a library of testing and characterization routines, as well as many of the processing tools that are typically needed for thorough evaluation and testing of image sensors.

2. CONTACT INFORMATION

The primary contact for information regarding sales, support and technical information is:

Jova Solutions
965 Mission Street Suite 600
San Francisco, CA 94103
415-348-1400
415-348-1414 fax

info@jovasolutions.com
http://www.jovasolutions.com

3. PROPRIETARY INFORMATION

This document contains information deemed proprietary. Information contained herein may be protected under patents, copyright, or by other lawful means. Use or reproduction of this document is restricted under the terms of the license.

3.1 SOFTWARE LICENSE

The product described within this document contains licensed software that is protected under copyright law. You may not reverse engineer, decompile, disassemble, modify, translate, make any attempt to copy or discover the source code of the software, or create derivate works from the software.

3.2 REFERENCED DOCUMENTS

Here are the documents related to the ISL-3200, which you may find useful:

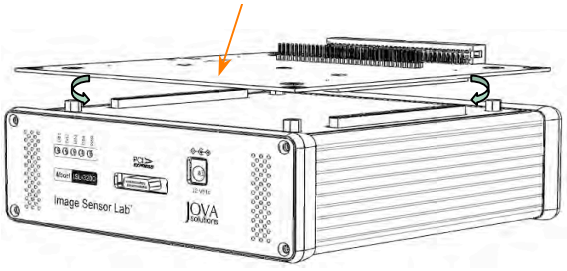
Description	*Doc. No*	*Company/Author*	*Rev. Date*
ISL-3200 Product Specification	210-0004-08	Jova Solutions	07/14/2009
ISL-3200 Basic User Manual	210-0001-08	Jova Solutions	07/14/2009
ISL-3200 Advanced Analysis Guide	210-0002-08	Jova Solutions	07/14/2009
ISL-3200 Quick Start Guide	210-0008-02	Jova Solutions	07/14/2009
ISL-3200 Test and Automation Suite Guide	210-0003-05	Jova Solutions	07/14/2009

4. HARDWARE FUNCTIONAL DESCRIPTION

4.1 OVERVIEW

160-pin high-density connectors

Customer-specific Adapter Board



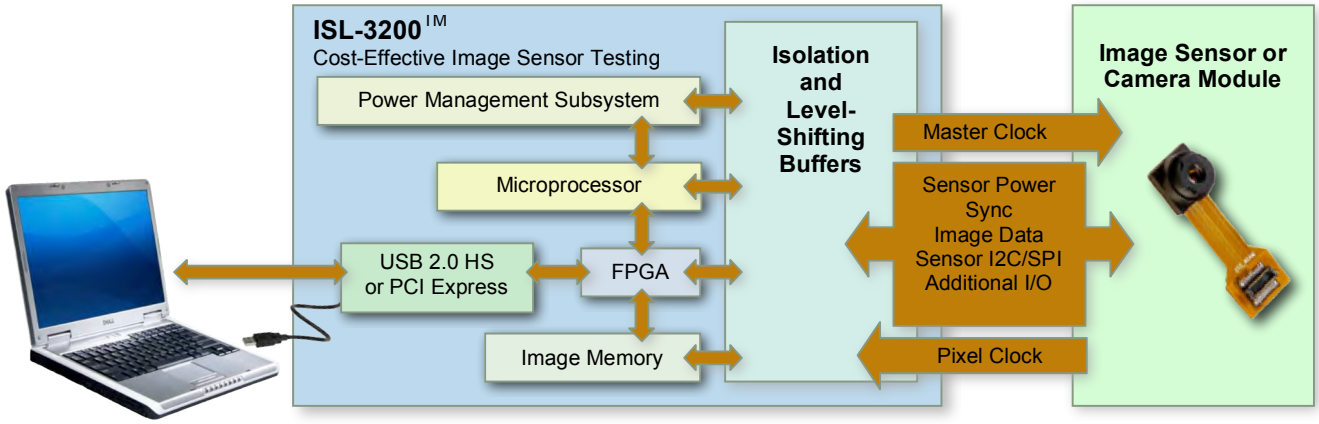
The Image Sensor Lab ISL-3200 is an electronic image sensor interface with built-in test and measurement capabilities. The ISL-3200 is a mixed signal device and includes programmable power supplies and oscillator, a flexible sensor image data frame capture capability. I2C, SPI, and UART sensor communication channels are also supplied.

- USB 2.0 HS Interface (450Mbps)
- Optional External PCIe (2.5 Gbps)
- Programmable power supplies with voltage and current measurement
- Programmable master clock oscillator up to 136 MHz
- 8 and 16 bit data capture into on-board memory
- 32 Mbytes on-board memory for USB version, 128 Mbytes for PCIe version
- Additional digital I/O
- I2C, SPI, and UART sensor communications provided
- Sensor signal voltage translation buffers with programmable isolation
- Built-in timer/counter
- Optional embedded Volt-Ohm Meter with 2x80 switch matrix (Short/Open test capable)
- Image Sensor Lab ISL-3200 Product Specification
- Drivers and automation API available

Image Sensors are typically connected to the ISL-3200 by a custom adapter board, which is mounted to the top of the ISL-3200, using the two 180-pin high density connectors, as shown in the figure above.

The ISL-3200 is housed in a compact 160mm x 160mm x 53 mm enclosure that is connected to the host computer via a USB 2.0 HS cable (or optional External PCIe cable).

A block diagram showing the major components of the ISL-3200 is shown below The image sensor is connected to internal circuitry through voltage level translation buffers in order to accommodate image sensors operating with different signal levels. An FPGA is used for the frame capture logic as well as the built-in timer/counter measurements. A microcontroller is also used within the ISL-3200 to control and coordinate the various devices, including the power management circuitry. A variety of power supplies is included with voltage and current measurement capability. A high-resolution current measurement mode is available for measuring standby currents in the µA range.



4.2 HARDWARE CONFIGURATION OPTIONS

The ISL-3200 if offered with two hardware-configuration options that are summarized in the table below.

Configuration Option	Description
PCIe	This option replaces the USB 2.0 HS interface to the much faster PCI Express interface between the ISL-3200 and the host computer. This upgrade also includes a more powerful FPGA and 128 Mbytes of on-board memory.
VOM	The VOM option adds Voltage and Resistance measurement capabilities in two instrument modes to support unpowered shorts/opens testing and signal voltage monitoring during powered testing. The DMM mode provides approximately 4-digit measurement resolution at sampling rates in the 1K-10K samples per second range. The VOM mode provides approximately 7-digit measurement resolution at sampling rates between 10-100 samples per second. The instrumentation is connected to various interface signals though an Analog Switch matrix in a 2x80 cross-point configuration (HI and LO probe vs 80 test points).

The table below shows the ISL-3200 model numbers for each combination of add-on options.

ISL Model	3203	3204	3207	3208
USB 2.0 HS	■	■		
External PCI Express (PCIe)			■	■
2-Wire VOM (Short/Open)		■		■

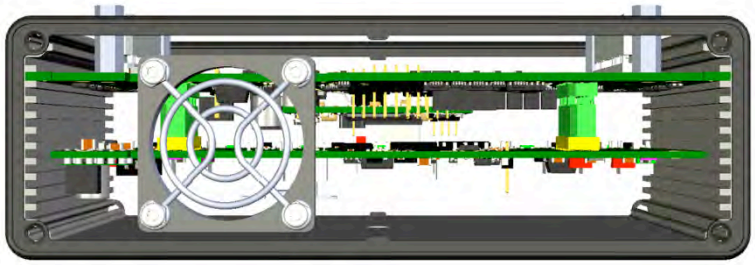
4.3 PHYSICAL DESCRIPTION

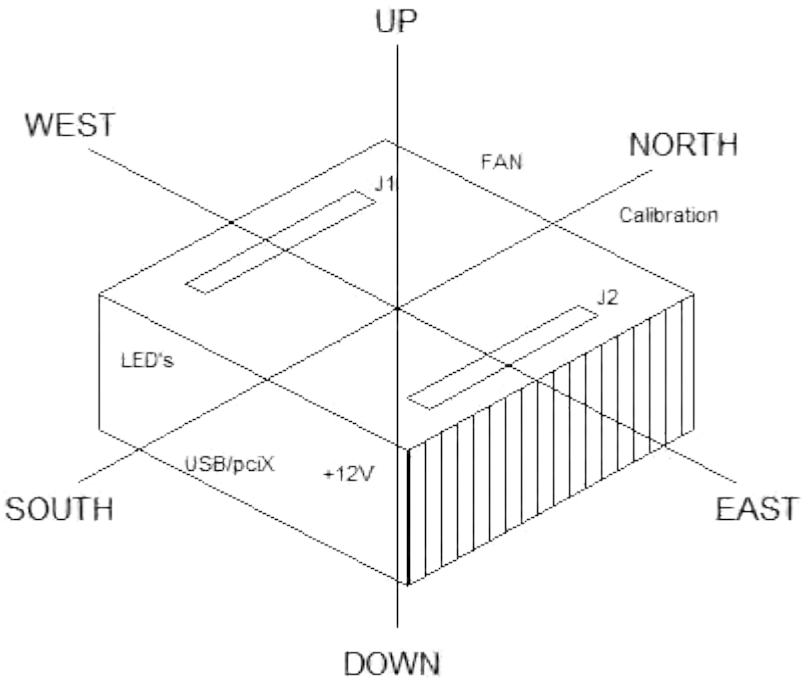
The ISL-3200 instrument is housed in a metal enclosure with connectors for power, communications, and image sensor connection. The overall size is 160mm wide by 160mm deep by 51mm high.

Two 180-pin high-density connectors on the top of the ISL-3200 are used for sensor power and interface signals.

The ISL-3200 is powered from an external +12VDC, 3 Amp minimum power source, via a 2.5mm center pin Power Plug (e.g., a 12V laptop style supply).

The ISL-3200 is controlled via a USB 2.0 High Speed Interface or the optional PCIe High Speed Interface.





4.4 TEST INTERFACE

The ISL-3200 Series Test Interface connections are detailed in the diagrams below.

J1			West
Signal	Pin	Pin	Signal
GND	2	1	GND
PSB_OUT	4	3	
PSB_RTN	6	5	
	8	7	ADPT_3V2_OUT
	10	9	ADPT_3V2_GND
PSD_OUT	12	11	PSF_OUT
PSD_RTN	14	13	PSF_RTN
	16	15	
	18	17	
GND	20	19	GND
LED_PWM2_OUT	22	21	PSH_OUT
LED_PWM2_RTN	24	23	PSH_RTN
BRITE_LED2_OUT	26	25	
BRITE_LED2_RTN	28	27	
	30	29	
RGB2_OUT	32	31	PWM2_OUT
RGB2_RED_RTN	34	33	PWM2_RTN
RGB2_GRN_RTN	36	35	PSY_OUT
RGB2_BLU_RTN	38	37	PSY_RTN
GND	40	39	GND
GND	42	41	GND
PSU_OUT	44	43	I2C_VREF
PSU_RTN	46	45	I2C_SCL_RES
PSU_OUT_Sense	48	47	I2C_SDA_RES
PSU_RTN_Sense	50	49	I2C_SCL
ABS_USER0	52	51	I2C_SDA
ABS_USER1	54	53	ADPT_I2C_SDA
ABS_USER2	56	55	ADPT_I2C_SCL
ABS_USER3	58	57	ADPT_I2C_VREF
GND	60	59	GND
ABS_PSU_OUT	62	61	REFCLK
ABS_PSU_RTN	64	63	PIXCLK
	66	65	PSIO
	68	67	
	70	69	
	72	71	UART_TX
	74	73	UART_RX
	76	75	UART_RTS
	78	77	UART_CTS
GND	80	79	GND
Continued			Pins 81 through 160 Next Page

J2			East
Signal	Pin	Pin	Signal
GND	2	1	GND
PSIO	4	3	PSA_OUT
PSIO	6	5	PSA_RTN
ADPT_3V1_OUT	8	7	
ADPT_3V1_GND	10	9	
PSE_OUT	12	11	PSC_OUT
PSE_RTN	14	13	PSC_RTN
	16	15	
	18	17	
GND	20	19	GND
PSG_OUT	22	21	LED_PWM1_OUT
PSG_RTN	24	23	LED_PWM1_RTN
	26	25	BRITE_LED1_OUT
	28	27	BRITE_LED1_RTN
	30	29	
PWM1_OUT	32	31	RGB1_OUT
PWM1_RTN	34	33	RGB1_RED_RTN
PSX OUT	36	35	RGB1_GRN_RTN
PSX RTN	38	37	RGB1_BLU_RTN
GND	40	39	GND
GND	42	41	GND
SPI_SCK	44	43	
SPI_SDO	46	45	
SPI_SDI	48	47	
SPI_nSS	50	49	
SPI_nCS0	52	51	
SPI_nCS1	54	53	
SPI_nCS2	56	55	
SPI_nCS3	58	57	
GND	60	59	GND
	62	61	
ADPT_SPI_nCS0	64	63	
ADPT_SPI_nCS1	66	65	
ADPT_SPI_nCS2	68	67	
ADPT_SPI_nCS3	70	69	
ADPT_SPI_nCS4	72	71	ADPT_SPI_nSS
ADPT_SPI_nCS5	74	73	ADPT_SPI_SDI
ADPT_SPI_nCS6	76	75	ADPT_SPI_SCK
ADPT_SPI_nCS7	78	77	ADPT_SPI_SDO
GND	80	79	GND
Continued			Pins 81 through 160 Next Page

Notes: Gray – Reserved for Future Use. Do Not Connect to these pins.
Yellow – Analog boundary scan test point.

J1 Cont.			West
Signal	Pin	Pin	Signal
GND	82	81	GND
	84	83	DIO_B0
	86	85	DIO_B1
	88	87	DIO_B2
	90	89	DIO_B3
	92	91	DIO_B4
	94	93	DIO_B5
	96	95	DIO_B6
	98	97	DIO_B7
GND	100	99	GND
	102	101	
	104	103	DIO_D0
	106	105	DIO_D1
	108	107	DIO_D2
	110	109	DIO_D3
	112	111	DIO_D4
	114	113	DIO_D5
	116	115	DIO_D6
	118	117	DIO_D7
GND	120	119	GND
GND	122	121	GND
	124	123	DIO_F0
	126	125	DIO_F1
	128	127	DIO_F2
	130	129	DIO_F3
	132	131	DIO_F4
	134	133	DIO_F5
	136	135	DIO_F6
	138	137	DIO_F7
GND	140	139	GND
	142	141	
	144	143	
	146	145	
	148	147	
	150	149	
	152	151	
	154	153	
	156	155	
	158	157	
GND	160	159	GND

J2 Cont.			East
Signal	Pin	Pin	Signal
GND	82	81	GND
DIO_A0	84	83	
DIO_A1	86	85	
DIO_A2	88	87	
DIO_A3	90	89	
DIO_A4	92	91	
DIO_A5	94	93	
DIO_A6	96	95	
DIO_A7	98	97	
GND	100	99	GND
	102	101	
DIO_C0	104	103	
DIO_C1	106	105	
DIO_C2	108	107	
DIO_C3	110	109	
DIO_C4	112	111	
DIO_C5	114	113	
DIO_C6	116	115	
DIO_C7	118	117	
GND	120	119	GND
GND	122	121	GND
DIO_E0	124	123	
DIO_E1	126	125	
DIO_E2	128	127	
DIO_E3	130	129	
DIO_E4	132	131	
DIO_E5	134	133	
DIO_E6	136	135	
DIO_E7	138	137	
GND	140	139	GND
	142	141	
	144	143	
	146	145	
	148	147	
	150	149	
	152	151	
	154	153	
	156	155	
	158	157	
GND	160	159	GND

Notes: Gray – Reserved for Future Use. Do Not Connect to these pins.
Yellow – Analog boundary scan test point.

4.4.1 ISL-3200 vs. ISL-1600 Compatibility Considerations

ISL-3200 power supplies PSA through PSD are similar in effective operating voltage range to an ISL-1600-PS01, however have half the maximum current.

In the ISL-1600, PSE, a PS01 type supply provides its output power to internal buffer circuitry as well, as being available for external use. In the ISL-3200, a separate PSIO supply provides power to internal buffers and is available as a voltage reference at the test interface. Other supplies that meet or exceed the PS01 type supply performance for most applications are available for use to provide PSE power.

The ISL-1600-PS03 type supply has been incorporated and is available as PSU.

To minimize ISL-1600 user efforts to transition to an ISL-3200 Series unit, an FPGA logic file is provided for use containing the ISL-1600 Capture Logic. The use of certain ISL-3200 signals are either fixed or prohibited.

The ISL-3200 Series Test Interface for ISL-1600 Compatibility is detailed in the diagrams below.

J1			West
Signal	Pin	Pin	Signal
GND	2	1	GND
PSB_OUT	4	3	
PSB_RTN	6	5	
	8	7	ADPT_3V2_OUT
	10	9	ADPT_3V2_GND
PSD_OUT	12	11	PSF_OUT
PSD_RTN	14	13	PSF_RTN
	16	15	
	18	17	
GND	20	19	GND
LED_PWM2_OUT	22	21	PSH_OUT
LED_PWM2_RTN	24	23	PSH_RTN
BRITE_LED2_OUT	26	25	
BRITE_LED2_RTN	28	27	
	30	29	
RGB2_OUT	32	31	PWM2_OUT
RGB2_RED_RTN	34	33	PWM2_RTN
RGB2_GRN_RTN	36	35	PSY_OUT
RGB2_BLU_RTN	38	37	PSY_RTN
GND	40	39	GND
GND	42	41	GND
PSU_OUT	44	43	I2C_VREF
PSU_RTN	46	45	I2C_SCL_RES
PSU_OUT_Sense	48	47	I2C_SDA_RES
PSU_RTN_Sense	50	49	I2C_SCL
ABS_USER0	52	51	I2C_SDA
ABS_USER1	54	53	ADPT_I2C_SDA
ABS_USER2	56	55	ADPT_I2C_SCL
ABS_USER3	58	57	ADPT_I2C_VREF
GND	60	59	GND
ABS_PSU_OUT	62	61	REFCLK
ABS_PSU_RTN	64	63	PIXCLK
	66	65	PSIO
	68	67	
	70	69	
	72	71	UART_TX
	74	73	UART_RX
	76	75	UART_RTS
	78	77	UART_CTS
GND	80	79	GND
Continued			Pins 81 through 160 Next Page

J2			East
Signal	Pin	Pin	Signal
GND	2	1	GND
PSIO	4	3	PSA_OUT
PSIO	6	5	PSA_RTN
ADPT_3V1_OUT	8	7	
ADPT_3V1_GND	10	9	
PSE_OUT	12	11	PSC_OUT
PSE_RTN	14	13	PSC_RTN
	16	15	
	18	17	
GND	20	19	GND
PSG_OUT	22	21	LED_PWM1_OUT
PSG_RTN	24	23	LED_PWM1_RTN
	26	25	BRITE_LED1_OUT
	28	27	BRITE_LED1_RTN
	30	29	
PWM1_OUT	32	31	RGB1_OUT
PWM1_RTN	34	33	RGB1_RED_RTN
PSX OUT	36	35	RGB1_GRN_RTN
PSX RTN	38	37	RGB1_BLU_RTN
GND	40	39	GND
GND	42	41	GND
SPI_SCK	44	43	
SPI_SDO	46	45	
SPI_SDI	48	47	
SPI_nSS	50	49	
SPI_nCS0	52	51	
SPI_nCS1	54	53	
SPI_nCS2	56	55	
SPI_nCS3	58	57	
GND	60	59	GND
	62	61	
ADPT_SPI_nCS0	64	63	
ADPT_SPI_nCS1	66	65	
ADPT_SPI_nCS2	68	67	
ADPT_SPI_nCS3	70	69	
ADPT_SPI_nCS4	72	71	ADPT_SPI_nSS
ADPT_SPI_nCS5	74	73	ADPT_SPI_SDI
ADPT_SPI_nCS6	76	75	ADPT_SPI_SCK
ADPT_SPI_nCS7	78	77	ADPT_SPI_SDO
GND	80	79	GND
Continued			Pins 81 through 160 Next Page

Notes: Gray – Reserved for Future Use. Do Not Connect to these pins.
Yellow – Analog boundary scan test point.

ISL-3200 Series Test Interface for ISL-1600 Compatibility, continued

J1 Cont.			West
Signal	Pin	Pin	Signal
GND	82	81	GND
	84	83	BOUT-0
	86	85	BOUT-1
	88	87	BOUT-2
	90	89	BOUT-3
	92	91	BIN-0
	94	93	BIN-1
	96	95	BIN-2
	98	97	BIN-3
GND	100	99	GND
	102	101	
	104	103	D0
	106	105	D1
	108	107	D2
	110	109	D3
	112	111	D4
	114	113	D5
	116	115	D6
	118	117	D7
GND	120	119	GND
GND	122	121	GND
	124	123	Hi-Z
	126	125	Hi-Z
	128	127	Hi-Z
	130	129	Hi-Z
	132	131	Hi-Z
	134	133	Hi-Z
	136	135	Hi-Z
	138	137	Hi-Z
GND	140	139	GND
	142	141	
	144	143	
	146	145	
	148	147	
	150	149	
	152	151	
	154	153	
	156	155	
	158	157	
GND	160	159	GND

J2 Cont.			East
Signal	Pin	Pin	Signal
GND	82	81	GND
VSYNC	84	83	
XSYNC-0	86	85	
XSYNC-1	88	87	
XSYNC-2	90	89	
Hi-Z	92	91	
Hi-Z	94	93	
Hi-Z	96	95	
Hi-Z	98	97	
GND	100	99	GND
	102	101	
D8	104	103	
D9	106	105	
D10	108	107	
D11	110	109	
D12	112	111	
D13	114	113	
D14	116	115	
D15	118	117	
GND	120	119	GND
GND	122	121	GND
Hi-Z	124	123	
Hi-Z	126	125	
Hi-Z	128	127	
Hi-Z	130	129	
Hi-Z	132	131	
Hi-Z	134	133	
Hi-Z	136	135	
Hi-Z	138	137	
GND	140	139	GND
	142	141	
	144	143	
	146	145	
	148	147	
	150	149	
	152	151	
	154	153	
	156	155	
	158	157	
GND	160	159	GND

Notes: Gray – Reserved for Future Use. Do Not Connect to these pins.
Yellow – Analog boundary scan test point.

4.5 HOST COMPUTER INTERFACE

The ISL-3200 default hardware configuration includes a USB 2.0 HS interface and is described below in paragraph 4.5.1. An optional External PCI Express interface is also available and comes as a replacement to the USB interface (i.e., one or the other, but not both).

4.5.1 USB 2.0 HS Interface

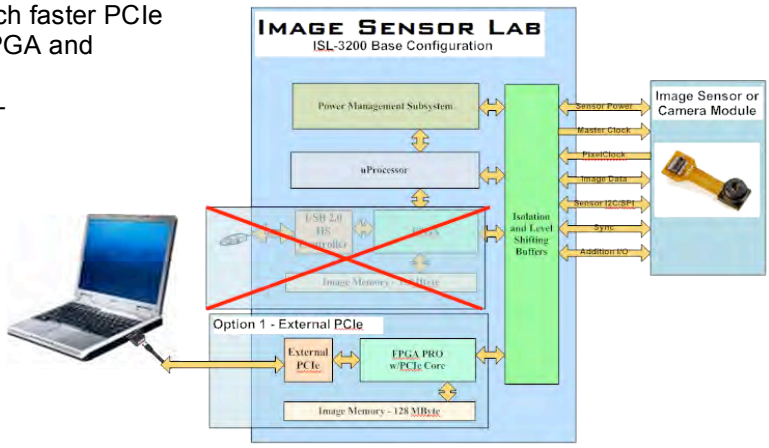
The USB is compliant with the USB.org specification revision 2.0 High-Speed requirements.

The ISL-3200 is a USB 'Self-Powered' device - it does not draw any power from the USB +5V line.

The USB ground signal line is tied to ISL-3200 common ground, external power adaptor DC return, and enclosure.

4.5.2 PCIe Interface

This option replaces the USB interface with a much faster PCIe interface, and provides a larger more powerful FPGA and 128MByte RAM for the image data buffer.
The PCIe interface uses a standard Molex 74150-0001 connector, which can be connected to the External PCIe connectors that are provided on most laptop computers. An inexpensive simple PCIe plug-in card is also available for desktop and workstation computers.



5. HARDWARE SPECIFICATIONS

5.1 INPUT POWER REQUIREMENTS

The ISL-3200 requires an external power source of +12V, 3 amps minimum.

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Voltage		11.5	12.0	12.5	VDC	
Current		3.0	4.0	5.0	A	
Ripple and Noise				1%	V (p-p)	
Load Regulation			5		%	
Line Regulation			5		%	

5.1.1 Input Power Connections

Module input power is provided through a 2.5mm ID, 5.5mm OD, center-pin positive receptacle.

Receptacle: CUI, Inc, PN: PJ-1028H (or equivalent)

+12VDC Center Pin
DC Return Outer Ring

External Power Supply

Example AC/DC Adaptors

SL Power Electronics (/Ault) PW153KB1203F01 for 3.4A
PW174KB1203F01 for 5.0A

5.2 OUTPUT POWER SPECIFICATION

5.2.1 Output Power Overview

Primary power for the Camera/Sensor and supporting Adaptor circuitry available are dependent on the presence of the optional Power Management Bundle and are detailed in the table below.

Name	Voltage	Current	Remote V-Sense	Analog Scan	CTRL Scan	Low Current	PS Type Source
PS-DIO	Off/1.25 - 4V 128-steps	100mA	(1)		Yes *V only*		LDO35
PS-A	Off/1.25 - 4V 128-steps	100mA	n/a (2)	Yes	Yes	Yes	LDO35
PS-B	Off/1.25 - 4V 128-steps	100mA	n/a (2)	Yes	Yes	Yes	LDO35
PS-C	Off/1.25 - 4V 128-steps	100mA	n/a (2)	Yes	Yes	Yes	LDO35
PS-D	Off/1.25 - 4V 128-steps	100mA	n/a (2)	Yes	Yes	Yes	LDO35
PS-E	Off/0.6 - 1.8V 31-steps	600mA	n/a (2)	Yes	Yes	Yes	SM1
PS-F	Off/0.6 - 1.8V 31-steps	600mA	n/a (2)	Yes	Yes	Yes	SM1
PS-G	Off/1.2 - 3.4V 31-steps	600mA	n/a (2)	Yes	Yes	Yes	SM2
PS-H	Off/1.2 - 3.4V 31-steps	600mA	n/a (2)	Yes	Yes	Yes	SM2
PS-U	0-10V 4096-steps	0-tbd (600) mA Current Limit Tbd-steps	Yes	Yes(3)	Yes	n/a(4)	Custom
PS-X	Off/1.25 - 3.3V 8 fixed steps	150mA					LDO12
PS-Y	Off/1.25 - 3.3V 8 fixed steps	150mA					LDO12
PS-ADPT-1	Off/3.3V	150mA					LDO0
PS-ADPT-2	Off/3.3V	150mA					LDO0
PWM1	Open Drain	150mA					PWM
PWM2	Open Drain	150mA					PWM
LED-PWM1	Open Drain	150mA					LED-PWM
LED-PWM2	Open Drain	150mA					LED-PWM
BRITE-LED1	29V max	500mA max					SM3
BRITE-LED2	29V max	500mA max					SM3
RGB-LED1 (3 output)	Open Drain	16.6mA					RGB-LED
RGB-LED2 (3 output)	Open Drain	16.6mA					RGB-LED

Notes:

(1) Capability Not Available
(2) Capability Not Currently Available –Signal Paths Reserved for Future Possible Upgrade
(3) PSU Analog Scan Option for Resistance Only – (see separate section)
(4) PSU Low Current Not Available -- Future Possible Capability

5.2.2 PSIO, PSA, PSB, PSC, PSD (1.25V – 3.8V, 100 mA)

- High-resolution low-frequency measurements of output voltage and current, and remote voltage sensing, are supported.
- Medium-resolution medium-frequency measurements of output voltage and current, and remote voltage sensing, are supported.

Note: For proper digital signal operation, both PSIO and PS wired for powering camera/sensor digital IO should be programmed to output the same voltage levels.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(LDO35)}$	Quiescent current, only one of LDO3, LDO4, LDO5 is enabled	$I_{O(LDO35)}$ = 0 (VIN_LDO35)			70		µA
$I_{O(LDO35)}$	Output current range					100	mA
$V_{O(LDO35)}$	LDO3, LDO4, LDO5 output voltage	Output Voltage, Selectable via I²C			Available output voltages: $V_{O(LDO35)TYP}$ = 1.224 V to 4.46 V, 25 mV steps		V
		Dropout voltage, 100-mA load				240	mV
		Total accuracy, 100 mA load $V_{(VIN\_LDO35)}$ = 5 V		–3%		3%	
		Load regulation, V(VIN_LDO35) > $V_{O(LDO35)TYP}$ + 0.5 V	load: 1 mA → 50 mA	–1%		1%	
		Line regulation, 10 mA load, V(VIN_LDO35): $V_{O(LDO35)TYP}$ + 0.5 V → 4.7 V		–1%		1%	
$I_{SC(LDO35)}$	Short circuit current limit	Output grounded			250		mA
$PSR_{(LDO35)}$	PSRR at 10 kHz	V(VIN_LDO35) > $V_{O(LDO3,5)}$ +1 V, 50 mA load at output			40		dB
$R_{DCH(LDO35)}$	Discharge resistor	LDO is disabled by I²C command			400		Ω
$I_{LKG(LDO35)}$	Leakage current	LDO off			1		µA

A mechanical relay, 50mOHMS max, is used for the output connect/disconnect (excluding PSIO).

5.2.3 PSE, PSF (0.6V – 1.8V, 600mA)

- High-resolution low-frequency measurements of output voltage and current, and remote voltage sense, are supported.
- Medium-resolution medium-frequency measurements of output voltage and current, and remote voltage sense, are supported.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(SM1)}$	Quiescent current for SM1	$I_{Q(SM1)}$ = I(VIN_ SM1), no output load	Not switching		10		µA
		SM1 OFF, set via I^2C			0.1		
$I_{O(SM1)}$	Output current range					600	mA
$V_{O(SM1)}$	Output voltage, PWM mode	Output voltage , selectable via I^2C, Standby OFF		Available output voltages: $V_{O(SM1)TYP}$ = 0.6 V to 1.8 V, adjustable in 40 mV steps			V
		$V_{O(SM1)}$ = $V_{SBY(SM1)}$, Output voltage range, Standby ON		Available output voltages: $V_{SBY(SM1)}$ = 0.6 V to 1.8 V, adjustable in 40 mV steps			
		Total accuracy, $V_{O(SM1)TYP}$ = $V_{SBY(SM1)}$ = 1.24 V, V(VIN_SM1) = 3.0 V to 4.7 V; 0 mA ≤ $I_{O(SM1)}$ ≤ 600 mA		–3%		3%	
		Line Regulation, V(VIN_SM1): 3.0 → 4.70 V, $I_{O(SM1)}$ = 10 mA			0.027		%/V
		Load Regulation, V(VIN_SM1) = 4.7 V, $I_{O(SM1)}$: 60 mA → 540 mA			0.139		%/A
$R_{DSON(PSM1)}$	P-channel MOSFET on-resistance	V(VIN_SM1) = 3.6 V, 100% duty cycle set			310	500	mΩ
$I_{LKG(PSM1)}$	P-channel leakage current				0.1		µA
$R_{DSON(NSM1)}$	N-channel MOSFET on-resistance	V(VIN_SM1) = 3.6 V, 0% duty cycle set			220	330	mΩ
$I_{LKG(PSM1)}$	N-channel leakage current				5		µA
$I_{LIM(SM1)}$	P&N -channel current limit	3.0 V < V(VIN_SM1) < 4.7 V		900	1050	1200	mA
$f_{S(SM1)}$	Oscillator frequency	PWM mode set		1.3	1.5	1.7	MHz
$EFF_{(SM1)}$	Efficiency	V(VIN_SM1) = 4.2 V, PWM mode, $I_{O(SM1)}$ = 300 mA, $V_{O(SM1)}$ = 3 V			90%		
$t_{SS(SM1)}$	Soft start ramp time	Converter OFF→ON, $V_{O(SM1)}$: 5% → 95% of target value			750		µs
$t_{DLY(SM1)}$	Converter turn-on delay	GPIO1 pin programmed as SM1 converter enable control. Measured from V(GPIO1): LO → HI			170		µ s

A mechanical relay, 50mOHMS max, is used for the output connect/disconnect.

5.2.4 PSG, PSH (1.0V – 3.4V, 600mA)

- High-resolution low-frequency measurements of output voltage and current, and remote voltage sense, are supported.
- Medium-resolution medium-frequency measurements of output voltage and current, and remote voltage sense, are supported.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(SM2)}$	Quiescent current for SM2	$I_{Q(SM2)}$ = I(VIN_ SM2), no output load	Not switching		10		µA
		SM2 OFF, set via I²C			0.1		
$I_{O(SM2)}$	Output current range					600	mA
$V_{O(SM2)}$	Output voltage	Output voltage , selectable via I²C, Standby OFF		Available output voltages: $V_{O(SM2)TYP}$ = 1.0 V to 3.4 V, adjustable in 80 mV steps			V
		$V_{O(SM2)}$ = $V_{SBY(SM2)}$, Output voltage range, Standby ON		Available output voltages: $V_{SBY(SM2)}$ = 1.0 V to 3.4 V, adjustable in 80 mV steps			
		Total accuracy, $V_{O(SM2)TYP}$ = $V_{SM2(SBY)}$ = 1.8 V, V(VIN_SM2) = greater of [3.0 V or ($V_{O(SM2)}$ + 0.3 V)] to 4.7 V; 0 mA ≤ $I_{O(SM2)}$≤ 600 mA		–3%		3%	
		Line regulation, V(VIN_SM2) = greater of [3.0 V or ($V_{O(SM2)}$ + 0.3 V)] to 4.7 V; 0 mA ≤ $I_{O(SM2)}$≤ 600 mA			0.027		%/V
		Load regulation, V(VIN_SM2) = 4.7 V, $I_{O(SM2)}$: 60 mA → 540 mA			0.139		%/A
$R_{DSON(PSM2)}$	P-channel MOSFET on-resistance	V(VIN_SM2) = 3.6 V, 100% duty cycle set			310	500	mΩ
$I_{LKG(PSM2)}$	P-channel leakage current				0.1		µA
$R_{DSON(NSM2)}$	N-channel MOSFET on-resistance	V(VIN_SM2) = 3.6 V, 0% duty cycle set			220	330	mΩ
$I_{LKG(PSM2)}$	N-channel leakage current				5		µA
$I_{LIM(SM2)}$	P&N -channel current limit	3.0 V < V(VIN_SM2) < 4.7 V		900	1050	1200	mA
$f_{S(SM2)}$	Oscillator frequency	PWM mode set		1.3	1.5	1.7	MHz
$EFF_{(SM2)}$	Efficiency	V(VIN_SM2) = 4.2 V, $I_{O(SM2)}$ = 300 mA, $V_{O(SM2)}$ = 3 V			90%		
$t_{SS(SM2)}$	Soft start ramp time	Converter OFF→ON, $V_{O(SM2)}$: 5% → 95% of target value			750		µs
$t_{DLY(SM2)}$	Converter turn-on delay	GPIO2 pin programmed as SM2 converter enable control. Measured from V(GPIO2): LO → HI			170		µs

A mechanical relay, 50mOHMS max, is used for the output connect/disconnect.

5.2.5 PSU (0V – 10V, 500mA)

- High-resolution low-frequency measurements of output voltage and current, and remote voltage sense, are supported.
- Medium-resolution medium-frequency measurements of output voltage and current, and remote voltage sense, are supported.

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Voltage		0	3-5	10.25 tbd	VDC	Regulated
Current		0		500	mA	Limited
Ripple and Noise Voltage Current			 250 50 400	 500 100 800	 uVp-p uVrms nArms	
Load Regulation			tbd			
Transient Response			tbd			
Voltage Programming Accuracy			+/- 2.0	+/- 5.0	mV	
Current Limit Programming Accuracy			100		uA	
Voltage Measurement Accuracy				+/- 6.0	mV	
Current Measurement Accuracy Fixed Offset		 0	 +/- 50	 100	 uA uA	

A mechanical relay, 50mOHMS max, is used for the output connect/disconnect.

This supply is similar in design to the ISL-1600 power supply model PS03.

Remote regulation voltage sense is available.

Note: The output voltage range of PSU exceeds the range of the VOM circuit during power-on and therefore cannot be directly measured through the Analog Switch Matrix with the VOM option.

5.2.6 PSX, PXY (1.224V – 3.3V, 150 mA)

- Voltage and Current Measurements are not supported.
- Output is not calibrated.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(LDO1,2)}$	Quiescent current, either LDO1 or LDO2 enabled, LDO0 disabled	$I_{Q(LDO1,2)}$ = I(VIN_LDO02)	$I_{(LDO1,2)}$ = –1 mA		15		µA
			$I_{(LDO1,2)}$ = –150 mA		160		
$I_{O(LDO1,2)}$	Output current range					150	mA
$V_{O(LDO1,2)}$	LDO1, LDO2 Output Voltage	Output Voltage, Selectable via I²C.			Available output voltages: $V_{O(LDO1,2)}$TYP = 1.25, 1.5, 1.8, 2.5, 2.85, 3, 3.2, 3.3		V
		Dropout voltage, 150 mA load				300	mV
		Total accuracy, V(VIN_LDO02) = 3.65 V		–3%		3%	
		Line Regulation, 100 mA load, V(VIN_LDO02): $V_{(LDO1,2)TYP}$ + 0.5 V → 4.7 V		–1%		1%	
		Load regulation, load: 10 mA → 150 mA V(VIN_LDO02) > $V_{O(LDO1,2)\ TYP}$ + 0.5V		–1.5%		1.5%	
$P_{SR(LDO12)}$	PSRR at 20 kHz	150mA load at output, V(VIN_LDO02) – $V_{O(LDO1,2)}$=1V			40		dB
$I_{SC(LDO1,2)}$	LDO1&2 short circuit current limit	Output grounded			300		mA
$R_{DCH(LDO1,2)}$	Discharge resistor	LDO disabled by I²C command			300		Ω
$I_{LKG(LDO1,2)}$	Leakage current	LDO off			2		µA

5.2.7 Adaptor Power Output 1 (+3.3V)

- Voltage and Current Measurements are not supported.
- Output is not calibrated.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(LDO0)}$	Quiescent current	Internally connected to VIN_LDO12 pin	I(LDO0) = –1 mA		15		µA
			I(LDO0) = –150 mA		160		
$I_{O(LDO0)}$	Output current range					150	mA
$V_{O(LDO0)}$	Output voltage	Fixed output voltage value			3.3		V
		Dropout voltage , I(LDO0) = –150 mA				300	mV
		Total accuracy		–3%		3%	
		Line regulation, V(OUT): $V_{O(LDO0)}$+ 0.5 → 4.7 V; I(LDO0) =– 100 mA		–1%		1%	
		Load regulation, I(LDO0) = –10 mA →– 150 mA		–1.5%		1.5%	
$PSR_{(LDO0)}$	PSRR at 20 kHz	150 mA load at output , V(VIN_LDO12) – $V_{O(LDO1,2)}$=1V			40		dB
$I_{SC(LDO0)}$	Short circuit current limit	V(LDO0) = 0 V			300		mA
$I_{LKG(LDO0)}$	Leakage current	LDO off			1		µA

5.2.8 Additional Power Management Outputs

- Voltage and Current Measurements are not supported.
- Outputs are not calibrated.

5.2.8.1 Adaptor 3.3V Output 2

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(LDO0)}$	Quiescent current	Internally connected to VIN_LDO12 pin	I(LDO0) = –1 mA		15		µA
			I(LDO0) = –150 mA		160		
$I_{O(LDO0)}$	Output current range					150	mA
$V_{O(LDO0)}$	Output voltage	Fixed output voltage value			3.3		V
		Dropout voltage , I(LDO0) = –150 mA				300	mV
		Total accuracy		–3%		3%	
		Line regulation, V(OUT): $V_{O(LDO0)}$+ 0.5 → 4.7 V, I(LDO0) = – 100 mA		–1%		1%	
		Load regulation, I(LDO0) = –10 mA →– 150 mA		–1.5%		1.5%	
$PSR_{(LDO0)}$	PSRR at 20 kHz	150 mA load at output , V(VIN_LDO12) – $V_{O(LDO1,2)}$=1V			40		dB
$I_{SC(LDO0)}$	Short circuit current limit	V(LDO0) = 0 V			300		mA
$I_{LK(I(LDO0)}$	Leakage current	LDO off			1		µA

5.2.8.2 PWM Open Drain Outputs 1 & 2

PWM DRIVER , PWM OPEN DRAIN OUTPUT					
$V_{OL(PWM)}$	Low level output voltage	I(PWM)= 150 mA		0.5	V
F_{PWM}	PWM driver frequency	Frequency range	Set via I^2C, F_{PWM} = 0.5/1/1.5/2/3/4.5/7.8/15.6		Hz
		Total accuracy, relative to selected value	-20%	+20%	
D_{PWM}	PWM driver duty cycle	Duty cycle range	D_{PWM} = 6.25% to 100%, set via I^2C, 6.25% minimum step		–

5.2.8.3 LED PWM Open Drain Outputs 1 & 2

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LED_PWM DRIVER, LED_PWM OPEN DRAIN OUTPUT							
D_{LEDPWM}	LED_PWM driver duty cycle	Duty cycle range			D_{LEDPWM} = 0% to 99.6%, set via I²C, 256 steps 0.4% minimum step		
$F_{REP(LEDPWM)}$	LED_PWM driver duty cycle pattern repetition rate	256 pulses within repetition rate time	SM3_LF_OSC = 0		122		Hz
			SM3_LF_OSC = 1		180		
$V_{OL(LEDPWM)}$	Low level output voltage	I(LED_PWM) = 150 mA				0.5	V
$V_{OH(LEDPWM)}$	High level output voltage					6	V

5.2.8.4 RGB LED Open Drain Outputs 1 & 2

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RGB DRIVER, RED/GREEN/BLUE OPEN DRAIN OUTPUTS							
$t_{FLASH(RGB)}$	Flashing period	Flashing period range			$t_{FLASH(RGB)}$ = 1 to 8 sec, set via I2C, 0.5 sec minimum step, 8 steps		sec
		Total accuracy		-20%		+20%	
$t_{FLASH(ON)}$	Flash on time	Flash on time range, value selectable by I²C			Set via I²C , $t_{FLASH(ON)}$ = 0.1/0.15/0.2/0.25/0.3/0.4/ 0.5/0.6 Sec		sec
		Total accuracy, relative to selected value		-20%		+20%	
D_{RGB}	Duty cycle	Duty cycle range, value selectable via I²C			D_{RGB} = 0% to 99.98%, set via I²C, 3.23% minimum step		
$I_{SINK(RGB)}$	RGB output sink current	V(RED) = V(GREEN) = V(BLUE) = 2 V, set via I2C RGB_ISET1,0	00 = (Driver set to OFF)				mA
			01 =	2.4	4	5.6	
			10 =	4.8	8	11.2	
			11 =	7	12	16.6	
$V_{OL(RGB)}$	Low level output voltage	Output low voltage, 8 mA load, RED/GREEN/BLUE PINS		0.3			V
$I_{LKG(RGB)}$	Output off leakage current	V(RED)=V(GREEN)=V(BLUE) = 4.7 V, all drivers disabled			1		µA

5.2.8.5 Bright White LED Driver Outputs 1 & 2

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
WHITE LED CONSTANT CURRENT DRIVER							
$V_{VIN(SM3)}$	Input Voltage range	V(OUT) = 3.3 V		3.0		4.7	V
V_{OVP3}	Output over-voltage trip	OVP detected at V(SM3) > V_{OVP3}		26.5	29	30	V
$V_{HYS(OVP3)}$	Output over-voltage hysteresis	OVP not detected at V(SM3) < V_{OVP3} – $V_{HYS(OVP3)}$			1.8		V
V_{SM3REF}	LED current sense threshold	LED current below regulation point at V(FB3) < V_{SM3REF}		244	252	260	mV
$I_{O(SM3)}$	LED current	Current range, Vin = 3.3 V, $I_{O(SM3)} = \frac{V(SM3REF)}{R_{FB3}}$		0		25	mA
		Total accuracy, $I_{O(SM3)}$ = 10mA		–10%		10%	
D_{SM3SW}	LED switch duty cycle	Duty cycle range		D_{SM3SW} = 0% to 99.6%, set via I²C, 256 steps, 0.4% minimum step			–
F_{REF_SM3}	LED switch duty cycle pattern repetition rate	256 pulses within repetition rate time	SM3_LF_OSC = 0		122		Hz
			SM3_LF_OSC = 1		183		
$R_{DSON(SM3SW)}$	LED switch MOSFET on-resistance	V(OUT)=3.6 V; I(SM3SW)=20 mA			1	2	Ω
$I_{LKG(SM3SW)}$	LED switch MOSFET leakage				1		µA
$R_{DSON(L3)}$	Power stage MOSFET on-resistance	V(OUT) = 3.6 V; I(L3) = 200 mA			300	600	mΩ
$I_{LKG(L3)}$	Power stage MOSFET leakage				1		µA
$I_{MAX(L3)}$	Power stage MOSFET current limit	3 V < V(OUT) < 4.7 V		400	500	600	mA

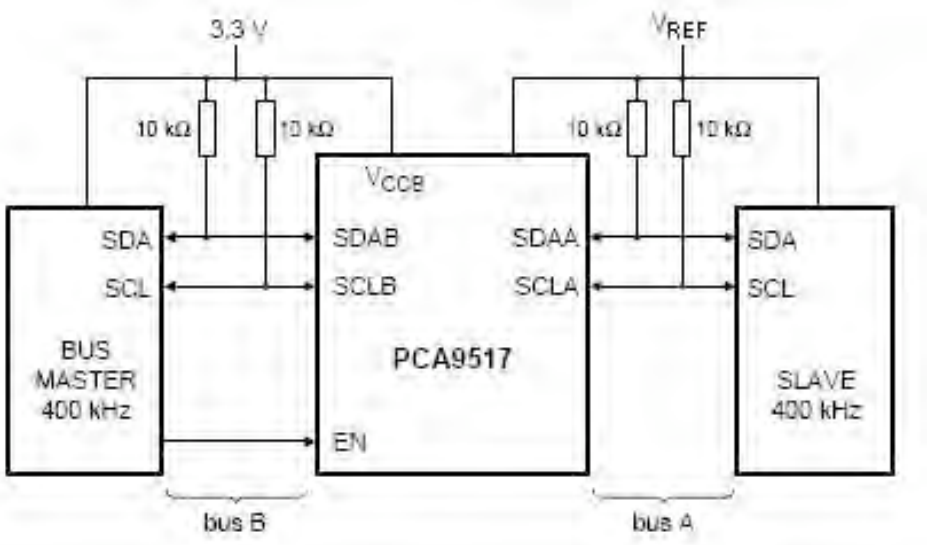
5.3 SENSOR COMMUNICATION

The ISL-3200 on-board processor provides I2C, SPI, and UART I/O to the connectors that can be passed through the adapter board to the image sensor.

5.3.1 I2C Bus Interface

The I2C signals SDA and SCL are bidirectional and open drain. These signals, therefore, require special considerations for signal termination to the digital IO voltage source.

The user must provide pull-up resistors of appropriate value, on the adaptor board assembly. The resistors should be placed between the I2C signal pull-up inputs to the ISL-3200 interface and the I2C VCC ref voltage input of the adaptor interface. The PSIO supply, or the desired PSA through PSH supplies, may be tied to the I2C VCC ref input, or other application specific power reference.



5.3.2 SPI Bus Interface

The Serial Peripheral Interface (SPI) sub-system supports full-duplex synchronous serial communications.

Primary features of the SPI sub-system are:

- Separate SPI signal pins for Camera/UUT and Adaptor use
- Camera SPI signal levels are variable with programmed setting of PSIO. (see paragraph 5.4)
- Adaptor SPI signal levels at 3.3v
- Four (4) Camera Chip Select Signals (negative true)
- Eight (8) Adaptor Chip Select Signals (negative true)
- SCK Frequency range, 39.0625 KHz to 20 MHz

5.3.3 UART Interface

The Universal Asynchronous Receiver Transmitter (UART) sub-system supports full-duplex serial communications, and can be configured to support hardware flow control via CTS and RTS signals.

Primary features of the UART sub-system are:

- Full-Duplex 8 or 9-bit transmission through TX and RX signal pins.
- Even, Odd or No Parity options (for 8-bit data).
- One or Two Stop bits.
- Hardware Flow Control option with CTS and RTS signal pins.
- UART Baud Rate range, 19.0735 bps to 5 Mbps.
- Parity, Framing Error Detection
- 1K Byte Receive Buffer
- 3.3V signal level standard, optional open drain with external pull up to up to 5V.

5.4 DIGITAL SIGNAL INTERFACE SPECIFICATION

All of the data and control signals to and from the image sensor are buffered with level-shifting, bi-directional, tri-state devices, providing proper voltage levels to the sensor and detection of the sensor's output levels.

Specification per Texas Instruments' SN74AVC4T245

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	1.2 V to 1.95 V		$V_{CCI} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.2 V to 1.95 V			$V_{CCI} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5)	1.2 V to 1.95 V		$V_{CCA} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5)	1.2 V to 1.95 V			$V_{CCA} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.1 V to 1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.1 V to 1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.7$ V, V_{IL} max = $V_{CCI} \times 0.3$ V.
(5) For V_{CC} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.7$ V, V_{IL} max = $V_{CCA} \times 0.3$ V.

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = −100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} − 0.2		V
		I_{OH} = −3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = −6 mA		1.4 V	1.4 V				1.05		
		I_{OH} = −8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = −9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = −12 mA		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.25				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	µA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±0.1	±1		±5	µA
				0 V to 3.6 V	0 V		±0.1	±1		±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V		±0.5	±2.5		±5	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					8	µA
				0 V	0 V to 3.6 V					−2	
				0 V to 3.6 V	0 V					8	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					8	µA
				0 V	0 V to 3.6 V					8	
				0 V to 3.6 V	0 V					−2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					16	µA
C_I	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		3.5			4.5	pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6			7	pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
t_{PHL}			2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	
t_{PLH}	B	A	2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	ns
t_{PHL}			2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	
t_{PZH}	$\overline{OE}$	A	3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	ns
t_{PZL}			3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	
t_{PZH}	$\overline{OE}$	B	3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns
t_{PZL}			3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	
t_{PHZ}	$\overline{OE}$	A	4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	ns
t_{PLZ}			4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	
t_{PHZ}	$\overline{OE}$	B	5.3	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	ns
t_{PLZ}			5.3	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	

5.4.1 Clocks

The Reference clock (REFCLK) source for the image sensor can come from one of three sources

- an on-board programmable oscillator clock (OSCCLK)
- an FPGA based clock derived from the oscillator clock
- an externally provided clock on the adapter circuitry

The Capture Clock (CAPCLK) can be either the Reference clock (REFCLK) going to the image sensor or the Pixel Clock (PIXCLK) coming from the image sensor.

5.4.1.1 Internal Clock Generation (OSCCLK and REFCLK)

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Oscillator Output Frequency (OSCCLK)		1.039 KHz		68.0254 MHz		OSCCLK
Total Frequency Accuracy			0.5	1.6	%	
Frequency Drift Over Temperature			10		ppm/ degree C	
Frequency Drift Over Supply			0.05		%/V	
Long Term Frequency Stability			300		ppm/ sqr kHr	
Timing Jitter			1		%	
Duty Cycle		49	50	51	%	
Maximum Useable Frequency				165.2 121.2 63.4	MHz MHz MHz	Design Range 3.3 V Design Range 2.5V Design Range 1.8V

5.4.1.2 Capture Clock “CAPCLK”

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Clock Input Frequency (PIXCLK or REFCLK) *note additional restriction from FPGA on frequency				165.2 150.3 116.9	MHz MHz MHz	Design Range 3.3 V Design Range 2.5V Design Range 1.8V
Duty Cycle		45	50	55	%	

5.4.2 Synchronization Signals

The ISL-3200 provides flexibility to configure the image frame capture logic for operation with most image sensor interface functions. The table below shows the frame capture configuration variables.

Frame Capture Configuration

Configuration Bit	Selection
Capture Clock	REFCLK or PIXCLK
Clock Edge	RISING or FALLING
Vsync Frame Start Edge	RISING or FALLING
Vsync Frame End Edge	RISING or FALLING
Xsync0 Gating	ENABLED or DISABLE
Xsync0 Gating State	HIGH or LOW
Xsync1 Gating	ENABLED or DISABLE
Xsync1 Gating State	HIGH or LOW
Xsync2 Gating	ENABLED or DISABLE
Xsync2 Gating State	HIGH or LOW

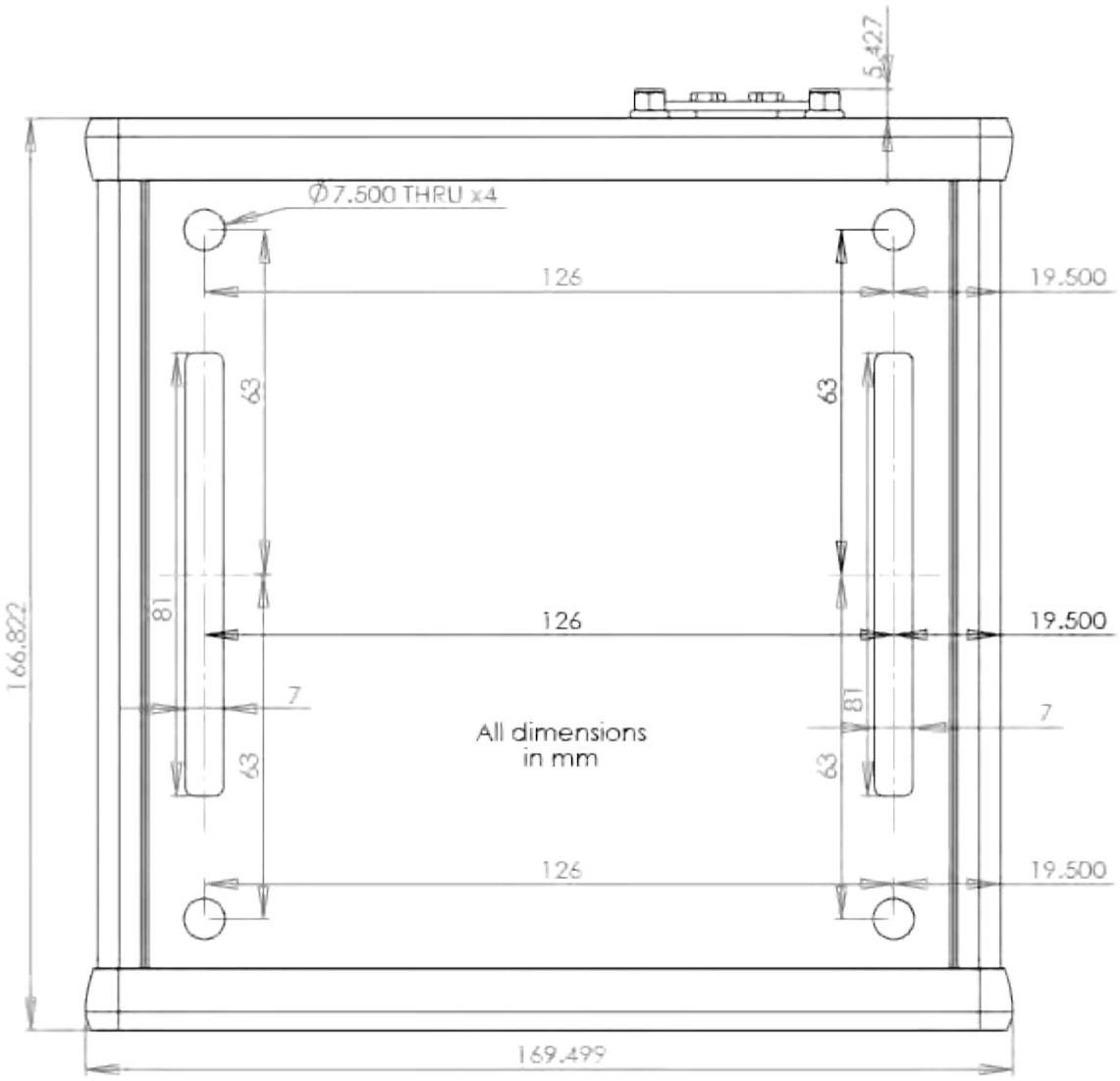
5.5 Static Digital Input and Output Control

Four (4) general-purpose digital inputs are available at the connector for connection from the image sensor. These lines can be used to receive shutter, LED, Motor or other digital signals from the image sensor. Logic detects and maintains a single change of state for each of these inputs, as well as providing live state status.

Four (4) general-purpose digital outputs are available at the connector for connection to the image sensor. These lines can be control the sensor RESET, CAPTURE or other sensor digital input.

5.6 MECHANICAL SPECIFICATIONS

5.6.1 Top Down View



Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Size Length Width Height			 160 160 51		 mm mm mm	 Excluding optional mounting brackets or feet.
Weight			32		Ounces	

5.7 CONNECTOR SPECIFICATIONS

Module input power is provided through a 2.5mm OD center pin receptacle.

Receptacle:	Switchcraft PN:	RAPC712	(or equivalent)
Pin-1	+12VDC	Center Pin	
Pin-2	DC Return	Outer Ring	

Input Power Mating Connector

Plug:	Switchcraft PN:	760
	CUI, Inc. PN:	PP3-002B

The ISL-3200 test interface connector pins are detailed in (paragraph 4.4). The mating connector (used on the adapter boards) is a SAMTEC QSE-080-01-F-D-A.

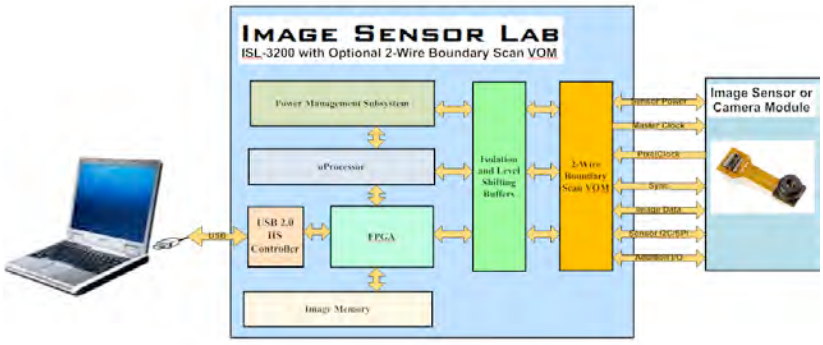
5.8 ENVIRONMENTAL SPECIFICATIONS

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Temperature		0		40	C	
Humidity				tbd	%	Non-Condensing
Altitude				10,000	ft	
Airflow						

5.9 VOM OPTION

5.9.1 Measurement Bus

The 2-Wire VOM option adds analog boundary scan capability with a HI_BUS and LO_BUS and programmable connections, through a 2x80 matrix of analog switches to the sensor signals and measurement instruments. The 2x80 configuration provides 2/4 wire access between instruments and the signals of the device under test.



5.9.1.1 2-Wire x 80 Analog Switch Matrix

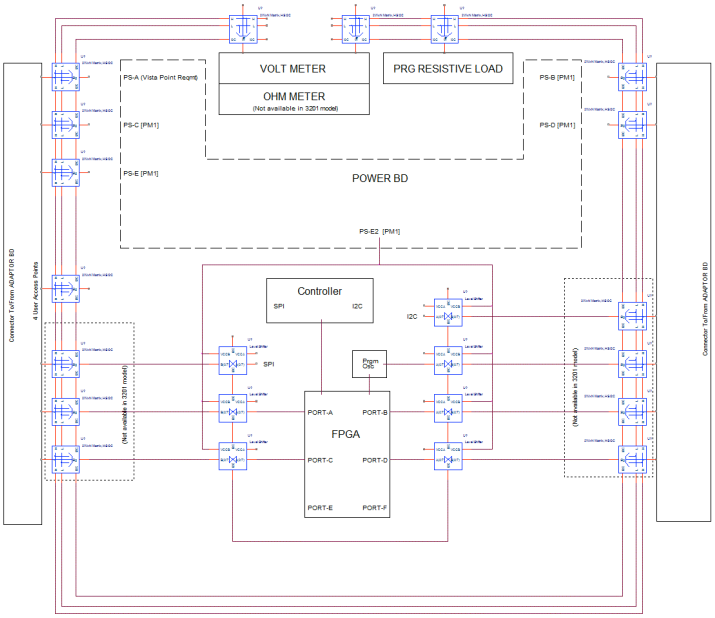
The Analog Devices' ADG791 series device is used for these analog switches.

Two instrument-probe-signals, referred to as the HI_Bus and LO_Bus, run the perimeter of the Signal Board.

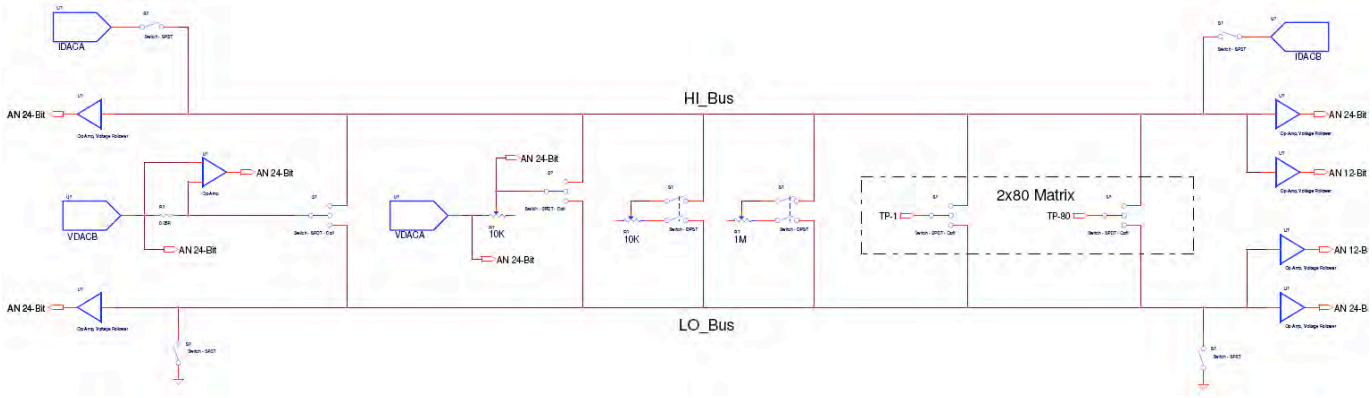
A series of 1x2 Analog Matrix Switches connect various instrumentation or test signals to either the HI_Bus or LO_Bus lines.

The VOM instrument signals are connected to the HI/LO Buses at each end of the Buses. All other instrumentation or test signals are connected between the ends.

Note: The voltage levels from PS-U exceed the limits of this matrix, therefore PS-U voltage will be measured separately. Mechanical relays are used to connect the PS-U to the HI_Bus or LO_Bus during power off ohms measurement (for shorts/opens testing).



5.9.2 Sources and Loads



5.9.2.1 Programmable Pull-Up Resistor Voltage Source -- VDACApu

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
VDACA						
Range		0		3.8	VDC	
Increment			1.22		mV	
Short-Circuit Current			30		mA	
Pull-Up						
POR Default			5.06k		Ohms	
Range		99.0625		10.06k		
Increment			39.0625			
Current				5	mA	

5.9.2.2 Programmable Pull-Up Resistor -- 10KPU

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
10K Pull-Up						
POR Default			5.06k		Ohms	
Range		99.0625		10.06k		
Increment			39.0625			
Current				5	mA	

5.9.2.3 Programmable Voltage Source with Current Measurement -- VDACB

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
VDACB						
Range		0		3.8	VDC	
Increment			1.22		mV	
Short-Circuit Current			30		mA	
Current Sense						Minimum target goals
Range		1u		30m	A	
Resolution			100n			

5.9.2.4 Programmable Current Sources – IDACA & IDACB

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
IDAC Range-1						
Range		2.0833		531.25	uA	
Increment			2.0833		uA	
Voltage				3.8	V	
						Open Circuit
IDAC Range-2						
Range		.004167		1.0625	mA	
Increment			4.167		uA	
Voltage				3.8	V	
						Open Circuit
IDAC Range-3						
Range		.008333		2.125	mA	
Increment			8.333		uA	
Voltage				3.8	V	
						Open Circuit

5.9.2.5 Programmable Resistive Loads -- 10Kohm and 1Mohm

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
10K Load						
POR Default			5.06k		Ohms	
Range		99.0625		10.06k		
Increment			39.0625			
Current				5	mA	
1M Load						
POR Default			500.06k		Ohms	
Range		3.96625k		1.0M		
Increment			3.90625K			
Current				500	uA	

5.9.3 Measurements

5.9.3.1 Voltage Measurements -- 12-bit and 24-bit VADC

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
12-Bit VADC						
Range		0		3.8	VDC	
Resolution			805		uV	
Sample Time (1000 points)				580	mSEC	[1]
Sample Time (100 points)				80		
24-Bit VADC						
Range		0		3.8	VDC	
Resolution			596		nV	
Sample Rate			30	32	Pts/Sec	[2]

Notes:

[1] Based on use of “DMM Measure HL_Bus Voltage.vi” with standard Sample & Hold and Conversion Period settings (as used during product calibration). Faster sample times can be achieved at the expense of less accuracy or increased sample point set noise.

[2] Based on use of standard ADC sampling settings (as used during product calibration). Faster sampling rates can be achieved at the expense of less accuracy or increased sample point set noise.

24-Bit ADC reading are continuously performed in the background and placed into circular storage buffers. Calls to return the contents of the circular buffer can be performed in less than 20ms. Calls to return new samples in the foreground (that is acquiring new samples not placed in the circular buffer) are returned at the sample rate.